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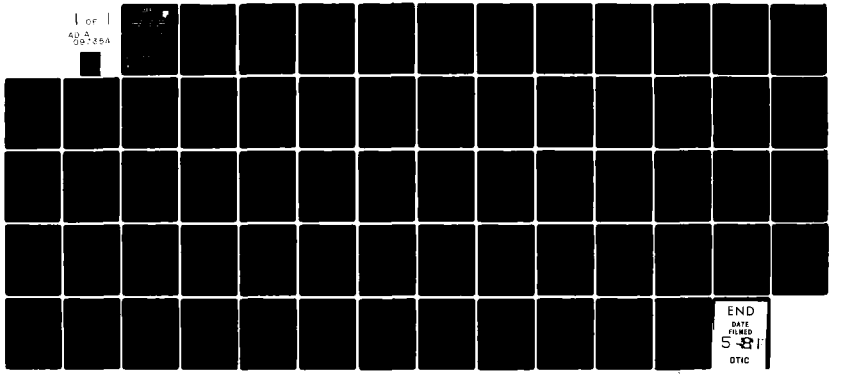

RADC-TR-80-408
In-House Report
February 1981

ACCESS PROTOCOL FOR A PARALLEL WIDEBAND LOCAL DIGITAL COMMUNICATION NETWORK (PROPOSED STANDARD)

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This report documents a proposed standard for an access protocol for interface to high capacity wideband general purpose data/communications busing system known as a "Flexible Intraconnect." An advanced development program is underway at RADC to design, fabricate, test and document a Flexible Intraconnect system. The objective of the development program is to prove the suitability of the Flexible Intraconnect (FI) bus technology as a standard approach to implementing military command, control and communica-

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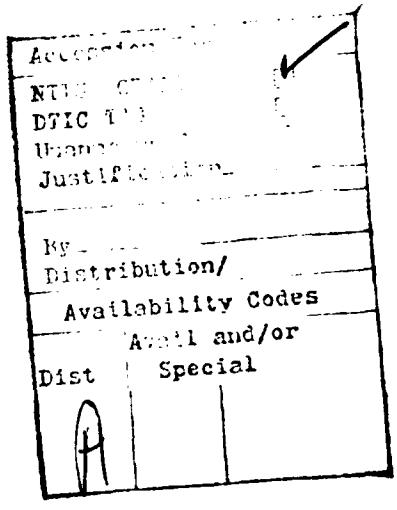
tions systems. Accordingly, documentation has been prepared describing technical characteristics and requirements of the FI. The FI System Specification No. SS07877940000 defines design parameters for the FI. A second document, called "MIL-STD-FI" describes the FI in terms of how to interface with and gain access to information distribution services provided by the FI.

This report contains the results of an in-house effort to define the access protocol to the Flexible Intraconnect. The work is presented in a form suitable for incorporation into a Military Standard.



PREFACE

This work was conducted under the Distributed C^2 thrust (R3C) of the Communications and Information Processing for C^2 section (RA3) of the RADC Technology Planning Objective (TPO) structure. Results of this effort have been incorporated in the Flexible Intraconnect Advanced Development Program.

ACKNOWLEDGMENT

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CONTENTS

INTRODUCTION

This report contains the results of an in-house effort to define and specify a standardized access protocol for a parallel wideband local digital communications network (Flexible Intraconnect System).

BACKGROUND

Considerable emphasis is now being placed on the development of superior command and control (C^2) capabilities for the Tactical Air Force. This is because C^2 is regarded as the "force multiplier", the critical equalizer against a numerically superior adversary. Achieving an effective C^2 capability and sustaining that capability once achieved, is a continuing challenge. Creating and maintaining a real C^2 advantage is a function of how quickly and effectively the benefits of new know-how and technology are integrated in operational military forces.

A Flexible Intraconnect (FI) capability is being developed to provide a uniform architecture upon which survivable modular C^2 centers may be quickly and economically developed; and once developed, be easily enhanced and rapidly adapted to meet dynamic mission requirements. The FI is a general purpose bus oriented communications network that provides information distribution services among member equipments[1]. Studies have been conducted[2,3] to determine the nature of information distribution services to be provided by the Flexible Intraconnect and to define (from a FI user's point of view)

equipment-to-FI interface in terms of physical, electrical, logical and functional characteristics. The information obtained from the interface studies was then organized and presented in a form suitable for incorporation into a military standard (MIL-STD).

TECHNICAL PROBLEM

The problem was to combine the results of engineering studies on the FI with other available technical data to form a document that describes the interface characteristics of the FI system. The interface standard applies to both communications as well as data processing equipments.

OBJECTIVE

The objective of this work was, therefore, to document technical interface requirements of a high capacity information distribution network.

DESCRIPTION OF INTERFACE PROTOCOL

The interface protocol defined in Appendix A is treated as three separate levels or "layers" of interfacing - physical, link and network. The layered protocol concept allows functional independence (transparancy) of information at each level.[4]

The physical layer describes word size, bit positions, bit designations and functions, and electrical requirements. In addition, the logic procedure for movement of words across the interface is specified. This procedure is a parallel word asynchronous balanced data transfer protocol, operating under the control of four logic signals.

The link interface describes data block format including header, header words, data fields and error control fields. Interpretation, limits, extensions and variations of these are defined.

The network interface describes procedures to implement address independent (packet) information distribution services.

Appendix A to this report "Input/Output Interfaces for the Flexible Intraconnect Bus System, Proposed MIL-STD-(FI)," presents the explicit technical requirements for device-to-bus protocols at the physical, link and network access levels for devices (Digital Terminal Equipments or DTEs) and the FI. The Appendix was prepared in a form suitable for eventual conversion to the Military Standardization Program.

REFERENCES

1. D.A. Griffith, "Flexible Intraconnect, A New Approach for Configuring Tactical Command and Control Centers," Proc. Local Area Communications Network Symposium, Boston MA, May 1979, pp. 263-277.

2. C. Schalbe, J. Powers, B. Chi, and G. Mayhew, "Modular C^3 Interface Analysis (Flexible Intraconnect)," RADC-TR-80-26, Rome Air Development Center, Griffiss AFB NY, March 1980. Vol 1, AD#B46390L, Vol 2, AD#B046391L.

3. W. Bedsole, and W. Kamsler, et al, "Modular C^3 Interface Analysis (Flexible Intraconnect)," RADC-TR-80-125, Rome Air Development Center, Griffiss AFB NY, April 1980. Vol 1, Part 1, AD#B049382L, Vol 1, Part 2, AD#B049383L, Vol 3, AD#B049384L.

4. International Organization for Standardization, "Reference Model of Open Systems Interconnection," ISO/TC 97/SC 16 W. Doc. N227, June 1979.

APPENDIX A

INPUT/OUTPUT INTERFACES

FOR THE

FLEXIBLE INTRACONNECT BUS SYSTEM

PROPOSED MIL-STD-(FI)

PROPOSED MIL-STD-(FI)(USAF)
11 December 1979

NOTE: This draft, dated 11 December 1979, prepared by Rome Air Development Center/DCLT has not been approved and is subject to modification.
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INPUT/OUTPUT INTERFACES

for the

Flexible Intraconnect Bus System

Department of the Air Force
Rome Air Development Center (AFSC)
Griffiss AFB, New York 13441

Input/Output Interfaces, Flexible Intraconnect Bus System, Air Force Systems

MIL-STD-(FI)(USAF)

1. This Military Standard is approved for use by Rome Air Development Center, Department of th Air Force, and is available for use by all Departments and Agencies of the Department of Defense.

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FOREWORD

1. This standard is intended for use by equipment designers and computer programmers as well as systems engineers and is limited to interface characteristics--physical, functional and electrical. This standard, by specifying functional interface requirements, does not specify the specific philosophy to be used for any system application; rather it is limited to functional characteristics of the interface signals and formats.

CONTENTS

1. SCOPE

1.1 Scope. This standard defines requirements for digital and analog input/output interfaces to the Flexible Intraconnect Bus System.

2. REFERENCED DOCUMENTS

2.1 Issues of Documents. The following documents of the issue in effect on date of invitation for bids or request for proposal, form a part of this standard to the extent specified herein.

MIL-M-38510/420-01, General Specification for Microcircuits

4. GENERAL STATEMENTS OF REQUIREMENTS

4.1 Interface Types. The Input/Output (I/O) interface requirements of the Flexible Intraconnect Bus System consist of two types: digital interfaces and analog interfaces.

4.1.1 Digital Interfaces. The I/O requirements specified herein include requirements for physical interface, link interface, and network interface for digital message blocks.

4.1.1.1 Digital Physical Interface. The I/O requirements include control and data signal definition and timing requirements for establishing and executing the transfer of a block of digital words.

4.1.1.2 Digital Link Interface. The I/O requirements include generation, definition, and interpretation of certain information within message block headers, message block data sections, and message block trailers.

4.1.1.3 Digital Network Interface. The I/O requirements include generation, definition, and interpretation of certain information within message block headers not defined in 4.1.1.2.

4.1.2 Analog Interfaces. The I/O requirements specified herein include frequency bands, channel formats and characteristics of analog channels.

5. DETAILED STATEMENTS OF REQUIREMENTS

5.1 Digital Interface.

5.1.1 Digital Physical Interface. The digital hardware interface is that combination of control and data signals that exists between a Digital Terminal Equipment (DTE) and the Flexible Intraconnect Bus (hereinafter referred to as "the Bus" or "Bus").

5.1.1.1 Interface Application. The digital hardware interface is intended to facilitate the transfer of digital information from a DTE to the Bus and from the Bus to a DTE.

5.1.1.2 Signal Lines. There shall be five control lines, eighteen data lines and one timing utility line. The direction of the data lines shall be determined by their usage, i.e., to transmit or receive data.

5.1.1.3 Line Configuration. The digital hardware interface shall be configured as shown in Figure 1.

5.1.1.4 Control Lines. The five control lines shall be designated as C1, C2, C3, C4 and C5. The logical signal designations for the control lines shall be as shown in Table I for data transfer from Bus to DTE. The logical signal designations for the control lines shall be as shown in Table II for data transfer from the DTE to the Bus.

5.1.1.5 Timing Utility Line. The timing utility line shall be designated as T1. The timing utility line shall be a unidirectional line carrying utility clock pulses from the Bus to the DTE. There is no expressed or implied function of the clock pulse signals within the scope of this standard. The frequency of the clock shall be 5.2567890 MHz (nominal) (see para 5.1.3.2 for more detail).

5.1.1.6 Data Lines. The eighteen data lines shall be designated as D0, D1, D2,...D17. The direction of all eighteen data lines shall be consistent among the lines. That is, data flow shall be permitted in either direction, i.e., bus to DTE or DTE to Bus, at any time but not in both directions at the same time. The data

lines shall use half-duplex operation. Lower numbered data lines shall be considered to be Least Significant Bits (LSB) and higher numbered data lines shall be considered to be Most Significant Bits (MSB).

5.1.1.7 Data Transmission Rate. The interface shall permit data transfer rates within the range of one tenth of a bit per second (0.1 bit/sec) nominal to ten million bits per second (10 Mb/s) nominal with respect to each of the data lines. The equivalent eighteen bit word parallel transfer range is from one tenth of a word per second to ten million words per second. The equivalent composite range of data transfer rates with respect to the eighteen data lines is 1.8 bits per second to 180 million bits per second (180 Mb/s).

5.1.1.8 Timing. Transfer with respect to data words shall be completely asynchronous.

5.1.1.9 Precedence of Direction. In the event both the Bus and the DTE wish to initiate a data transfer at the same time, the Bus shall prevail.

5.1.1.10 Data Transfer Procedure. Data shall be transferred across the interface in blocks. Transfer of data shall be conducted in accordance with a sequence of logical states of the control signals C1, C2, C3, and C4. The sequence of states of the four control signals shall be as shown in Figures 2, 3, 4, and 5. Figures 2 and 3 depict the sequence of control signal states applicable to the transfer of information from the Bus to the DTE. Figures 4 and 5 depict the sequence of control signal states applicable to the transfer of data from the DTE to the Bus.

5.1.1.11 Control Signal Direction. The direction of the control signals C1 and C2 shall be unidirectional. The direction of control signals C3, C4, and C5 shall be bidirectional. The logical name of the signal shall be determined based on the direction of data transfer. These names shall be as shown in Tables I and II.

5.1.1.12 Electrical Requirements. Electrical requirements for the interface circuits defined in 5.1.1 are specified herein. The interface shall be compatible with Transistor Transistor Logic (TTL), having logic levels in accordance with MIL-M-38510/420-01 POP, General Specification for Microcircuits. All lines shall be tri-state, i.e., three possible output

states--two normal low-impedance logic "1" or "0" states and a high-impedance state that allows up to 128 tri-state outputs to be tied together and connected to a common bus line. In the high impedance state, maximum current leakage shall be no greater than 40 microamperes with 5.5 Vdc applied to the output. Figure 6 is a schematic representation of the electrical interface. Figure 7 is a figure of the interface electrical waveshape. Voltages shall be as shown in Table III.

5.1.2 Digital Link Interface. Data message block transfers across the I/O interface shall consist of a block of words containing a header section, a data section, and a trailer section in that order.

5.1.2.1 Interface Header Section The interface header section shall consist of sixteen words and each header word shall be eighteen bits wide. The bits in each word of the header shall be referred to as bit 0, bit 1,...bit 17 where bit 0 is the least significant bit and bit 17 is the most signficant bit.

5.1.2.1.1 Header Word Formats. The first fifteen words of the header shall consist of two nine bit halfwords. Bits 0 through 8 define the least significant halfword. Bits 9 through 17 define the most significant halfword. In each halfword the most significant bit shall be a latitudinal odd parity bit, that is, bit 8 is the parity bit for the least significant halfword and bit 17 is the parity bit for the most significant halfword. The last (sixteenth) word of the header shall be longitudinal odd parity of the first fifteen header words.

5.1.2.1.2 Header Field Formats. The header shall consist of fields. The header fields shall not include bit 8 or bit 17 of the header words. The format, definition, word position, interpretation, and constraints applicable to each header field shall be as described below. The notation used below follows these conventions:

Fields are designated by a string of identical characters.

Each character represents one bit of the header word/field.

The right-most symbol represents the least significant bit.

The left-most symbol represents the most significant bit.

All unused bit positions are designated by the character "/" and shall be set equal to 0 (zero).

The letter "p" designates latitudinal parity bits.

5.1.2.1.2.1 Word One. Word one of the header shall have the following format and interpretation:

p gggg aqqq p rrvv vvvv

Field	Bit Position	Definition
g	13-16	Message type
a	12	ACK/NACK mode
q	9-11	System mode
r	6-7	Message priority
v	0-5	Subbus number

qqqq field	Interpretation
0010	Local broadcast messages
0011	External broadcast messages
0100	Command messages (from DTE)
0101	Command messages (from Bus)
0110	Discrete messages
1010	Subbus message, virtual bus
1100	Subbus message, ring bus

a field	Interpretation
0	ACK/NACK procedure disabled
1	ACK/NACK procedure enabled

rr field	Interpretation
00	Lowest priority
01	Next to lowest priority
10	Next to highest priority
11	Highest priority

qqq field	Only value permitted is 000
vvvvvv field	Value 000000 not permitted

5.1.2.1.2.2 Word Two. Word two of the header shall have the following format and definition:

p u/ww wwww p //xx xxxx

Field	Bit Position	Definition
u	17	Virtual/real selector (0 = virtual, 1 = real)
w	9-14	Destination virtual address, high order
x	0-5	Destination virtual address, low order

All values are permitted for each field except only all zeros is used with Command Messages from the DTE, i.e., gggg (message type) field equal to 0100.

5.1.2.1.2.3 Word Three. Word three of the header shall have the following format, definition and interpretation:

p //yy yyyy p ffzz zzzz

Field	Bit Position	Definition
y	9-14	Destination real address (high order)
f	6-7	Header interpretation flag
z	0-5	Destination real address (low order)

Fields y and z are each permitted all values except 000000.

Field ff	Interpretation
Bit 6	Bit Set = 1 only by DTE when DTE is sending and indicating header interpretation is necessary
Bit 7	Bit Set = 1 only by Bus when Bus is sending and indicating header interpretation is necessary.

5.1.2.1.2.4 Word Four. Word four of the header shall have the following format and definition:

p //jj jjjj p //kk kkkk

Field	Bit Position	Definition
j	9-14	Source virtual address, high order
k	0-5	Source virtual address, low order

All values permitted for each field except 000000 is only used with Command Messages from the Bus, i.e., gggg (message type) field equal to 0101.

5.1.2.1.2.5 Word Five. Word five of the header shall have the following format, definition and interpretation:

p //11 1111 p ddmm mmmm

Field	Bit Position	Definition
l	9-14	Source real address, high order
d	6-7	Data block sizing code
m	0-5	Source real address, low order

Fields l and m are each permitted all values except 000000.

Field dd	Interpretation
00	Data block length is not longer than 40 full words
01	Data block length is not longer than 1024 full words
10	Data block length is not longer than 2048 full words
11	Data block length is 4096 full words

5.1.2.1.2.6 Word Six. Word six of the header shall have the following format, definition and interpretation.

p cccc cccc p ccch bbbb

Field	Bit Position	Definition
c	9-16	Data word (full word) count (upper portion)
c	5-7	Data word (full word) count (lower portion)
h	4	Halfword indicator
b	0-3	Halfword bit count

Field h	Interpretation
0	Least significant halfword (bits 0 through 8) of last data word (following last full word) is not included
1	Both halfwords are included in last word of data (following last full word)

Field bbbb Value indicates number of least significant bits included in last halfword included in the last data word (following the last full word).

The total number of bits in the data section of the message block shall, therefore, be represented by the following expression: (c x 18) + (h x 9) + (b) where c, h and b are the decimal equivalents of the binary values of each of the three fields. Refer to Table IV for a representative list of values for these fields.

5.1.2.1.2.7 Word Seven. Word seven of the header shall have the following format and definition:

p nnnn nnnn p nnnn nnnn

Field	Bit Position	Definition
n	9-16	Message number (upper portion)
n	0-7	Message number (lower portion)

5.1.2.1.2.8 Word Eight. Word eight of the header shall have the following format and definition.

p ssss ssss p ssss ssss

Field	Bit Position	Definition
s	9-16	Sequence number (upper portion)
s	0-7	Sequence number (lower portion)

5.1.2.1.2.9 Word Nine. Word nine of the header shall have the following format and definition:

p //// //// p //// tttt

Field	Bit Position	Definition
t	0-3	System time (high order bits of a 52 bit system time field)

5.1.2.1.2.10 Word Ten. Word ten of the header shall have the following format and definition:

p tttt tttt p tttt tttt

Field	Bit Position	Definition
t	9-16	System time (portion of 52 bit field)
t	0-7	System time (portion of 52 bit field)

5.1.2.1.2.11 Word Eleven. Word eleven of the header shall have the following format and definition:

p tttt tttt p tttt tttt

Field	Bit Position	Definition
t	9-16	System time (portion of 52 bit field)
t	0-7	System time (portion of 52 bit field)

5.1.2.1.2.12 Word Twelve. Word twelve of the header shall have the following format and definition:

p tttt tttt p tttt tttt

Field	Bit Position	Definition
t	9-16	System time (portion of 52 bit field)
t	0-7	System time (portion of 52 bit field)

5.1.2.1.2.13 Words Thirteen through Fifteen. Words thirteen, fourteen, and fifteen of the header shall have the following format and definition:

p //// //// p //// ////

5.1.2.1.2.14 Word Sixteen. Word sixteen of the header shall have the following format and definition:

e eeee eeee e eeee eeee

Word sixteen shall be a longitudinal (vertical) odd parity of the first fifteen words of the header.

5.1.2.1.2.15 Header Map. Figure 8 is a composite map of the header, illustrating field locations and codes.

5.1.2.1.3 Relationship to Digital Physical Interface. With the exception of control line C5 (see para 5.1.1.4), there is no relationship between the Digital Network Interface and the Digital Physical Interface. The relationship between control line C5 and the header shall be as follows:

Word 3 field f bit 6 is associated with transfer from the DTE to the Bus. C5 shall reflect the logical state of bit 6 during the period of message block transfer. Word 3 field f bit 7 is associated with transfer from the Bus to the DTE. C5 shall reflect the logical state of bit 7 during the period of message block transfer.

5.1.2.2 Data Section. The data section shall follow the header section and shall have the following limitations, constraints and conventions.

5.1.2.2.1 Data Section Size. The data section shall be defined in terms of numbers of data words as follows:

Type	Range (inclusive) (Number of words)
00	0 - 40
01	0 - 1024
10	0 - 2048
11	4096

In types 00, 01, and 10 the last word may consist of either one or two halfwords with the final halfword consisting of any number of bits from 1 to 9. Unused bits shall be the bits of lesser significance.

5.1.2.2.2 Word Definition. A standard data word is defined as an eighteen bit word. The bits in the standard data word shall be referred to as bit 0, bit 1,...bit 17 where bit 0 is the least significant and bit seventeen is the most significant bit. The number of words permitted in the data section shall be as described in 5.1.2.2.1.

5.1.2.2.2.1 Preferred Subsets. The following data word subsets shall be defined as preferred subsets. The preferred defined subsets are: a 16 bit subset, an 18 bit subset, and a 9 bit subset. The bit positions for these preferred word subsets shall be as shown below. "B" indicates used bit position, "/" indicates unused bit position.

Bit Position

	MSB															LSB
Preferred subset	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
16 bit subset	/	B	B	B	B	B	B	B	B	/	B	B	B	B	B	B	B	B
8 bit subset	/	/	/	/	/	/	/	/	/	/	B	B	B	B	B	B	B	B
9 bit subset	/	/	/	/	/	/	/	/	B	/	B	B	B	B	B	B	B	B

For the purposes of establishing word count, each word subset shall count as one word.

5.1.2.3 Trailer Section. The trailer section of the message block shall follow the data section and shall consist of eight words. The eight words shall consist of vertical odd parity bits based on the contents of the data section. The eight parity words shall be applied uniformly to the overall data section where each of the parity words is associated with approximately one eighth of the words in the data section. The first parity word in the trailer shall be the first word to follow the last word of the data section. The first word of the trailer shall be associated with the first eighth of the data section, the second word of the trailer shall be associated with the second eighth of the data section, etc. The eighth word of the trailer shall be associated with the last (remaining) "eighth" of the data section. The actual number of words in the last "eighth" of the data section may be more than the true arithmetic value of one-eighth of the total number of data words. In the event the number of data words in the data section is not evenly divisible by eight, the number of words contained in the final "eighth" shall be equal to the numerical equivalent obtained by dividing the total number of words in the data section by eight and adding the remainder. For example:

Total number of words = 747
Divided by 8 = 93, remainder = 3

In this case, the first seven parity (trailer) words would each be applied to each of the seven corresponding sets of 93 words in the data section. The last (eighth) trailer word would apply to the last set of 93 words plus the 3 remaining data words (total of 98 words in last "one-eighth" of the data section).

5.1.2.3.1 Very Short Blocks. For blocks with a data section of less than eight words, the eight trailer words shall be evenly distributed against the data words. For example, if the data section contained seven words, the first seven parity words would each be associated with each of the data words one through seven. The eighth parity word would be associated with word one. Or if the data section contained four words, the first and fifth parity words would each be associated with the first data word, the second and sixth parity words would each be associated with the second data word, etc. Or if there were only one data word, each of the eight parity words would be associated with the one data word. The allocation for all cases (from zero words through 7 words) is shown in Figure 4.

5.1.2.3.2 Data Word Subsets. The parity words in the trailer shall follow the same subset conventions used in the data section. That is if the data words are using the nine bit subset the parity words in the trailer shall be nine bit words.

5.1.2.3.2 Unused Data Bits. If the last word (or word subset) in the data section has unused bits, these bits shall be considered as equal to zero for purposes of computing the associated vertical parity trailer word.

5.1.2.4 Data Message Block Format. Figure 8 illustrates the composition of the complete message block for the digital link interface.

5.1.2.5 Order of Presentation. The message block shall be presented in the following order: header section followed by the data section followed by the trailer section. Within each section, words shall be presented in natural sequence, i.e., word one of the header is the first word to be presented. In the event that individual words are not presented in full parallel style, the most significant halfword shall be presented first. In the event that complete halfwords are not fully presented in parallel, the bits shall be presented in the order of most significant bits followed by lesser significant bits in descending order.

5.1.3 Digital Network Interface. The network interface protocol relates to the interpretation of information transferred across the standard interface. Transfers of information across the interface shall be constructed as shown in Figure 10.

5.1.3.1 Header Interpretation by Message Type. Interpretation and contents of certain fields of the header section shall depend on the contents of the message type field (bits 13-16, word one) of the header section of the message block.

5.1.3.1.1 Local Broadcast Messages. Message type code 0010 shall define a Local Broadcast message. There are no fields that require special interpretation for a local broadcast message. The following fields have no function for local broadcast messages:

Field	Code/Size/ Position		Definition
a	1	W1,B12	ACK/NACK
s	16	W8	Sequence number
v	6	W1	Subbus number
x	6	W2	Destination virtual address (low)
z	6	W3	Destination real address (low)

Fields x and z shall be set = to 111 111.

5.1.3.1.2 External Broadcast Messages. Message type code 0011 shall define an External Broadcast message. There are no fields that require special interpretation for anexternal broadcast message. The following fields have no function for external broadcast messages:

Field Code/Size/ Position			Definition
a	1	W1,B12	ACK/NACK
s	16	W8	Sequence number
u	1	W2	Virtual/real indicator
v	6	W1	Subbus number
w	6	W3	Destination virtual address (high)
x	6	W3	Destination virtual address (low)
y	6	W4	Destination real address (high)
z	6	W4	Destination real address (low)

Fields w, x, y and z shall each be set = to 111 111.

5.1.3.1.3 Command Message from DTE. Message type code 0100 shall define a command message from DTE. There are no header fields that require special interpretation for a command message from the DTE message. (Data interpretation is required and described in 5.1.3.2). The following fields are constrained as indicated below:

Field Code/Size/ Position			Constraint
w	6	W2	Destination virtual address (high) shall be 000000 (a pseudo address).
x	6	W2	Destination virtual address (low) shall be 000000.

5.1.3.1.4 Command Message from Bus. Message type code 0101 shall define a command message from the Bus message. There are no header fields that require special interpretation for a command message from the Bus message. (Data interpretation is required and described in 5.1.3.2). The following fields are constrained as indicated below:

Field Code/Size/ Position			Constraint
y	6	W3	Source virtual address (high) shall be 000000 (a pseudo address).
z	6	W3	Source virtual address (low) shall be 000000.

5.1.3.1.5 Discrete Messages. Message type code 0110 shall define a discrete (point-to-point) message. There are no fields that require special interpretation for a discrete message.

5.1.3.1.6 Subbus Message - Virtual Bus. Message type code 1010 shall define a Subbus Message - Virtual Bus. (The Virtual Bus (VB) is also known as a passive subbus.) The following header fields shall be interpreted as described below:

Field	Code/Size/ Position	
v	6 W1	The subbus number shall be used to identify one of sixty-three unique VB subbuses within the overall FI bus structure. The VB subbus number is used as a common address reference by those DTEs that are members of a particular subbus (virtual bus).
s	16 W8	The VB sequence number shall be used to indicate order of transmission on a virtual bus. The sequence number has no interpretation for non-transmitting members of a virtual bus. Interpretation of the VB sequence number is dependent on whether a particular subbus (virtual bus) is operating in mode A or mode B. In Virtual bus mode A, members of the bus shall transmit message blocks in a strict preestablished sequential order. The VB sequence number shall be used to determine the order in which each member of a virtual bus is to transmit. The VB sequence number shall be incremented by one count at each transmission. During initialization of a virtual bus each transmitting member is provided with three numbers: (1) A start up (initial) sequnce number, (2) A repetition interval, and (4) A wait time. As a VB begins operation, each member compares the received header VB sequence number to its assigned start up sequence number. If the two numbers match, the member is obligated to provide the next transmission on the VB. The transmission is delayed by the member until the wait time has been counted. The wait time is the amount of time a member must hold its transmission following receipt of its enabling sequence number. For example, if VB rember "M" is assigned start up sequence number = 17 and repetition interval = 20, M will transmit following receipt of VB message block header with sequence numbers 17, 37, 57, 77,.... (Choice and assignment of the initial sequence number, repetition interval, and wait time are accomplished at a higher level protocol outside the FI system.)

In virtual bus mode B, the transmit order and transmit enabling rate shall be regulated by a protocol established by the

members of a VB. The header sequence number is not used. In VP mode B, members transmit at quasi-periodic times based on control information provided by one member, designated as the VB "master." Individual members calculate time for transmission by the algorithm to + n(ti) +/- correction (t zero plus n times t sub i + or - correction), where to = original assigned time, ti = time interval between transmission, and correction = time difference provided by the VB master. The bus quantifies time to one microsecond for the purpose of regulating VB mode B operation.

5.1.3.1.7 Subbus Message - Lazy Susan Bus. Message type code 1100 shall define a subbus message - Lazy Susan Bus. (The Lazy Susan (LS) bus is also known as an active subbus or virtual ring in that each member of a LS subbus is obligated to accept a message block from the member preceding it in the ring. In the VB, or passive subbus, there is no obligation on any member to accept message blocks from other members.) The following header fields shall be interpreted as described below.

Field Code/Size/ Position			
v	6	W1	The subbus number shall be used to identify one of sixty-three unique LS subbuses within the overall FI bus structure. The LS subbus number is used as a common address reference by those DTEs that are members of a particular subbus (Lazy Susan).

Field Code/Size/ Position			
j	6	W4	The source virtual address (j = high, k = low) is used for queuing sequence of transmission among members of a LS subbus. When a LS subbus is established, one master is designated for the subbus. The participating members are identified as to their position on th LS ring. Device sequence is based on the source virtual address of the device which precedes it in the ring. Therefore, each member of the LS subbus is assigned a number that corresponds to the source virtual address of its predecessor in the ring. (Each member is also assigned a wait time. The wait time is the amount of time a member must delay transmission following receipt of a message block from its designated predecessor.)
k	6	W4	

5.1.3.2 Header Interpretation - General. The header words shall be interpreted as follows:

Field code/Size/ Position		
t	52 W9-W12	System time. System time is entered by the bus at the time a message block is released for transmission on the FI network. System time is measured from the beginning of the first day of the month of January, year 1900. The least significant digit of the system time field shall represent 2**16 picoseconds (65536 psec) which corresponds to a clock rate for the least significant digit (word 12 Bit 0) of the system time field of 15.25878906 MHz. This yields a clock rate at bit 4 word 12 of the system time field of 1.048576 MHz.

List of Tables and Figures

TABLE I. Control Lines Designations

for

Data Transfer from Bus to DTE.

Control Line Reference No.	Name of Line	Direction of Signal	Function of Signal
C1	Bus Output Request (BOR)	Bus to DTE	Set condition indicates bus system wants to transfer data block to DTE
C2	Not used (See Table II)	--	--
C3	Bus Data Available (BDA)	Bus to DTE	Set condition indicates a bus data word is available (for acceptance by DTE)
C4	DTE Receiver Ready (DRR)	DTE to Bus	Set condition indicates DTE is ready to accept a data word from bus
C5	Bus Mode Flag (BMF)	Bus to DTE	Set condition indicates interpretation is required within DTE

TABLE II. Control Line Designations

for

Data Transfer from DTE to Bus

Control Line Reference No.	Name of Line	Direction of Signal	Function of Signal
C1	Not used (See Table I)	--	--
C2	DTE Output Request (DOR)	DTE to Bus	Set condition indicates readiness of DTE to transfer data block to Bus system.
C3	DTE Data Available (DDA)	DTE to Bus	Set condition indicates DTE data word is available (for acceptance by Bus)
C4	Bus Receiver Ready (BRR)	Bus to DTE	Set condition indicates DTE ready to accept a data word from DTE.
C5	DTE Mode Flag (DMF)	DTE to Bus	Set condition indicates interpretation is required within Bus system.

TABLE III. TTL Compatible Voltages (Nominal)

NOMINAL VOLTAGE, V_T	OUTPUT CURRENT, I_T
Logic 0: 0 Vdc to 0.7 Vdc	2 ma
Logic 1: 2.7 Vdc to 5.5 Vdc	-0.4 ma
V_T Max: 7 Vdc, - .30 Vdc	
Tri-State High Impedance State	
Max Current Leakage: +/- 40 ua with a V_T of 5.5 Vdc	

TABLE IV. Representative Values for Header Word Six.

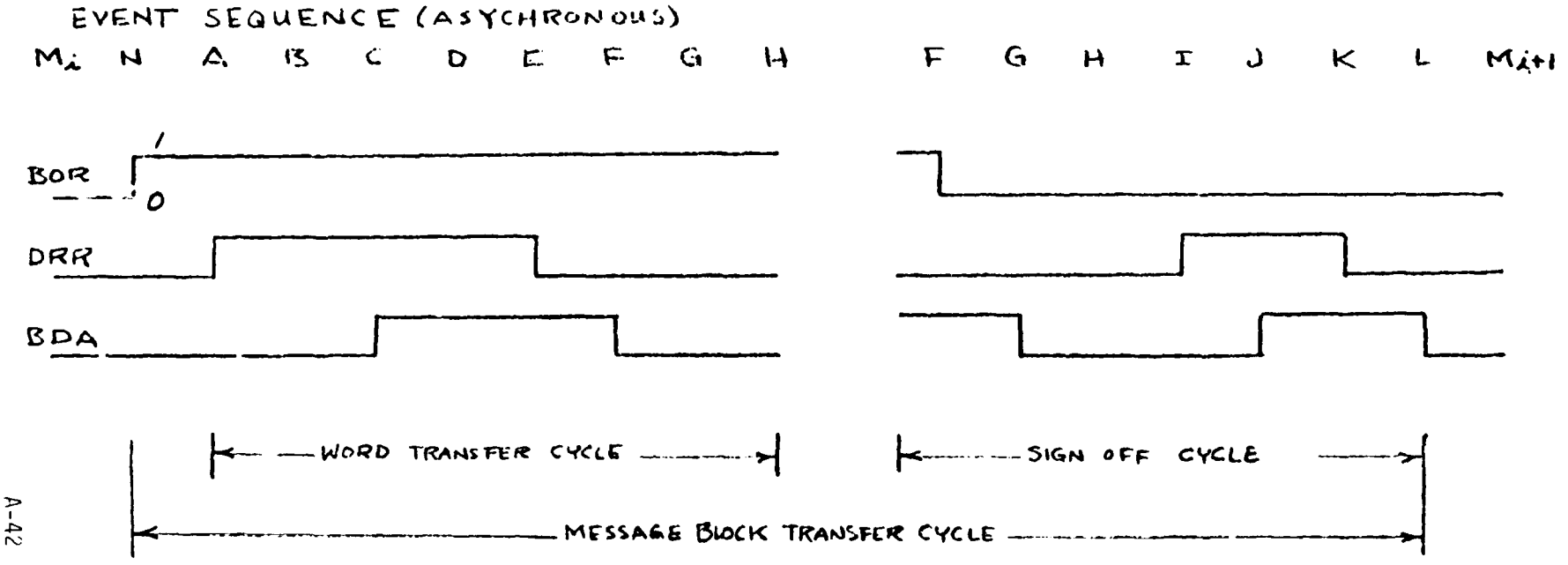
No. of Full Words	No. Bits in Partial Word	Binary Value of Register "c" (11 bits)	"h" (1 bit)	"b" (4 bits)
0	0	0	0	0
1	0	1	0	0
2	0	2	0	0
2047	0	2047	0	0
2048	0	2047	1	9
0	1	0	0	1
0	2	0	0	2
0	9	0	0	9
0	10	0	1	1
0	17	0	1	8
1	1	1	0	1
1	2	1	0	2
1	9	1	1	0
1	10	1	1	1
1	17	1	1	8

Signal Line Number	Line Name
D0	Data Line No. 1
D1	" " " 2
D2	" " " 3
D3	" " " 4
D4	" " " 5
D5	" " " 6
D6	" " " 7
D7	" " " 8
D8	" " " 9
D9	" " " 10
D10	" " " 11
D11	" " " 12
D12	" " " 13
D13	" " " 14
D14	" " " 15
D15	" " " 16
D16	" " " 17
D17	Data Line No. 18
C1	Control Line No. 1
C2	" " " 2
C3	" " " 3
C4	" " " 4
C5	Control Line No. 5
T1	Timing Utility Line

FIGURE 1. Digital Hardware Interface.

EVENT	SIGNAL LINE STATE: BOR C1	DOR C2	BDA C3	DRR C4	ACTION/INTERPRETATION
M(i)	0	0	0	0	Quiescent
N	1	0	0	0	Bus initiates data transfer cycle
A	1	0	0	1	DTE indicates ready for one word
B	1	0	0	1	Bus puts data word on data lines
C	1	0	1	1	Bus indicates data word is on lines
D	1	0	1	1	DTE accepts data word
E	1	0	1	0	DTE indicates busy with current word
F	1	0	1	0	Bus indicates there is another word (C1=1)
C	1	0	0	0	Bus indicates current word transfer complete
H	1	0	0	0	Return to event A for next word
F	0	0	1	0	Bus indicates no more words (C1-0)
G	0	0	0	0	Bus indicates current word transfer complete
H	0	0	0	0	DTE enters QUIT sequence
I	0	0	0	1	DTE indicates ready to quit
J	0	0	1	1	Bus indicates ready to quit
K	0	0	1	0	DTE signs off
L	0	0	0	0	Bus signs off (data transfer cycle complete)
M(i+1)	0	0	0	0	Quiescent

FIGURE 2. Block Data Transfer Procedure - Bus to DTE.

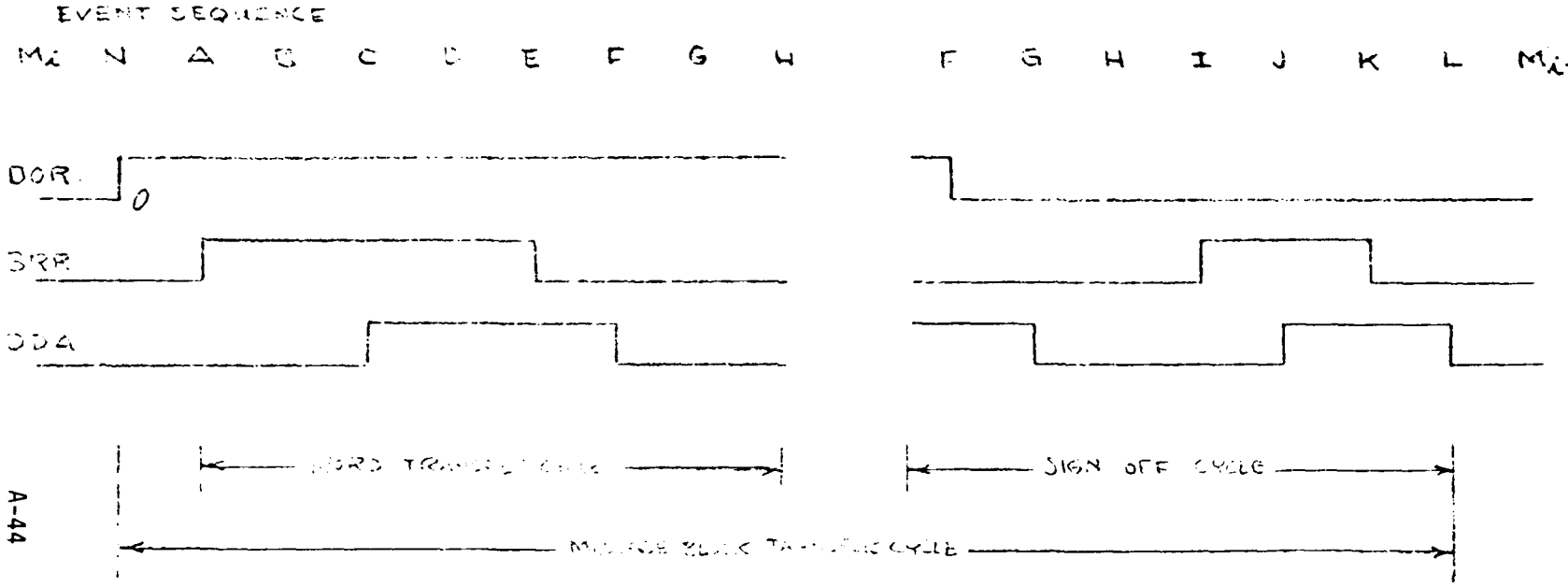


BOR Bus Output Request
DRR DTE Receiver Ready
BDA Bus Data Available

FIGURE 3. BLOCK DATA TRANSFER PROCEDURE - BUS TO DTE

	SIGNAL LINE STATE				
EVENT	BOR C1	DOR C2	DDA C3	BRR C4	ACTION/INTERPRETATION
M(i)	0	0	0	0	Quiescent
N	0	1	0	0	DTE initiates data block transfer cycle
A	0	1	1	0	Bus indicates ready for one word
B	0	1	1	0	DTE puts data word on data lines
C	0	1	1	1	DTE indicates data word is on lines
D	0	1	1	1	Bus accepts data word
E	0	1	0	1	Bus indicates busy with current word
F	0	1	0	1	DTE indicates there is another word (C2=1)
G	0	1	0	0	DTE indicates current word transfer complete
H	0	1	0	0	Return to event A for next word
F	0	0	0	1	DTE indicates no more words (C2-0)
G	0	0	0	0	DTE indicates current word transfer complete
H	0	0	0	0	Bus enters QUIT sequence
I	0	0	1	0	Bus indicates ready to quit
J	0	0	1	1	DTE indicates ready to quit
K	0	0	0	1	Bus signs off
L	0	0	0	0	DTE signs off (data block transfer cycle complete)
M(i+1)	0	0	0	0	Quiescent

FIGURE 4. Block Data Transfer Procedure - DTE to Bus.



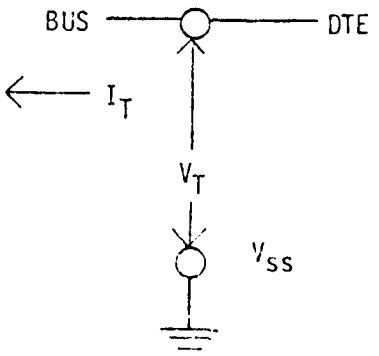
DOR DTE OUTPUT READY

SIRR DTE REQUEST

DDA DTE DATA AVAILABLE

FIGURE 5. BLOCK DATA TRANSFER

FOR [illegible] - DTE TO DCE



I_T Output Current

V_T Logic Voltage

V_{SS} Ground Reference Voltage and Logic Reference Zero

FIGURE 6. Electrical Interface.

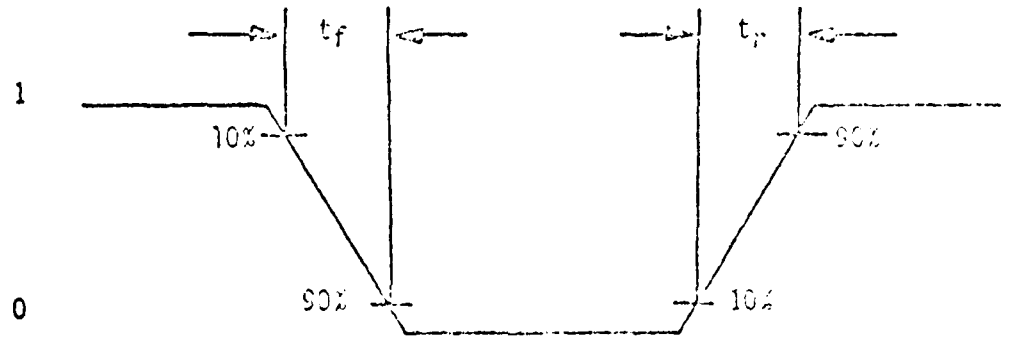


FIGURE 7. Interface Waveshape.

Header Word	Bit Position/Field Code																	
	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	p	g	g	g	g	a	q	q	q	p	r	r	v	v	v	v	v	v
2	p	u	/	w	w	w	w	w	w	p	/	/	x	x	x	x	x	x
3	p	/	/	y	y	y	y	y	y	p	f	f	z	z	z	z	z	z
4	p	/	/	j	j	j	j	j	j	p	/	/	k	k	k	k	k	k
5	p	/	/	l	l	l	l	l	l	p	d	d	m	m	m	m	m	m
6	p	c	c	c	c	c	c	c	c	p	c	c	c	h	b	b	b	b
7	p	n	n	n	n	n	n	n	n	p	n	n	n	n	n	n	n	n
8	p	s	s	s	s	s	s	s	s	p	s	s	s	s	s	s	s	s
9	p	/	/	/	/	/	/	/	/	p	/	/	/	/	t	t	t	t
10	p	t	t	t	t	t	t	t	t	p	t	t	t	t	t	t	t	t
11	p	t	t	t	t	t	t	t	t	p	t	t	t	t	t	t	t	t
12	p	t	t	t	t	t	t	t	t	p	t	t	t	t	t	t	t	t
13	p	/	/	/	/	/	/	/	/	p	/	/	/	/	/	/	/	/
14	p	/	/	/	/	/	/	/	/	p	/	/	/	/	/	/	/	/
15	p	/	/	/	/	/	/	/	/	p	/	/	/	/	/	/	/	/
16	e	e	e	e	e	e	e	e	e	e	e	e	e	e	e	e	e	e

Field	Size	Definition	Field	Size	Definition
a	1	ACK/NACK mode	n	6	message number
b	4	unused bit count	p	1	lat parity (1/2 wd)
c	11	word count	q	3	system mode
d	2	block sizing code	r	2	priority
e	18	longit parity	s	16	subbus seq no
f	2	header interpret	t	52	system time
g	4	message type	u	1	virtual/real ind
h	1	half word ind	v	6	subbus number
j	6	source virtual address (high)	w	6	destination virtual address (high)
k	6	source virtual address (low)	x	6	destination virtual address (low)
l	6	source real address (high)	y	6	destination real address (high)
m	6	source real address (low)	z	6	destination real address (low)
			/	-	unused bit position

FIGURE 8. Message Header Map and Field Codes.

Data Word	Trailer Word(s)
1	1, 8
2	2
3	3
4	4
5	5
6	6
7	7
1	1, 7
2	2, 8
3	3
4	4
5	5
6	6
1	1, 6
2	2, 7
3	3, 8
4	4
5	5

Data Word	Trailer Words
1	1, 5
2	2, 6
3	3, 7
4	4, 8
1	1, 4, 7
2	2, 5, 8
3	3, 6
1	1, 3, 5, 7
2	2, 4, 6, 8
1	1,2,3,4,5,6,7,8
0	All trailer words are set = to all ones

FIGURE 9. Allocation of Trailer Words to Less Than Eight Data Words

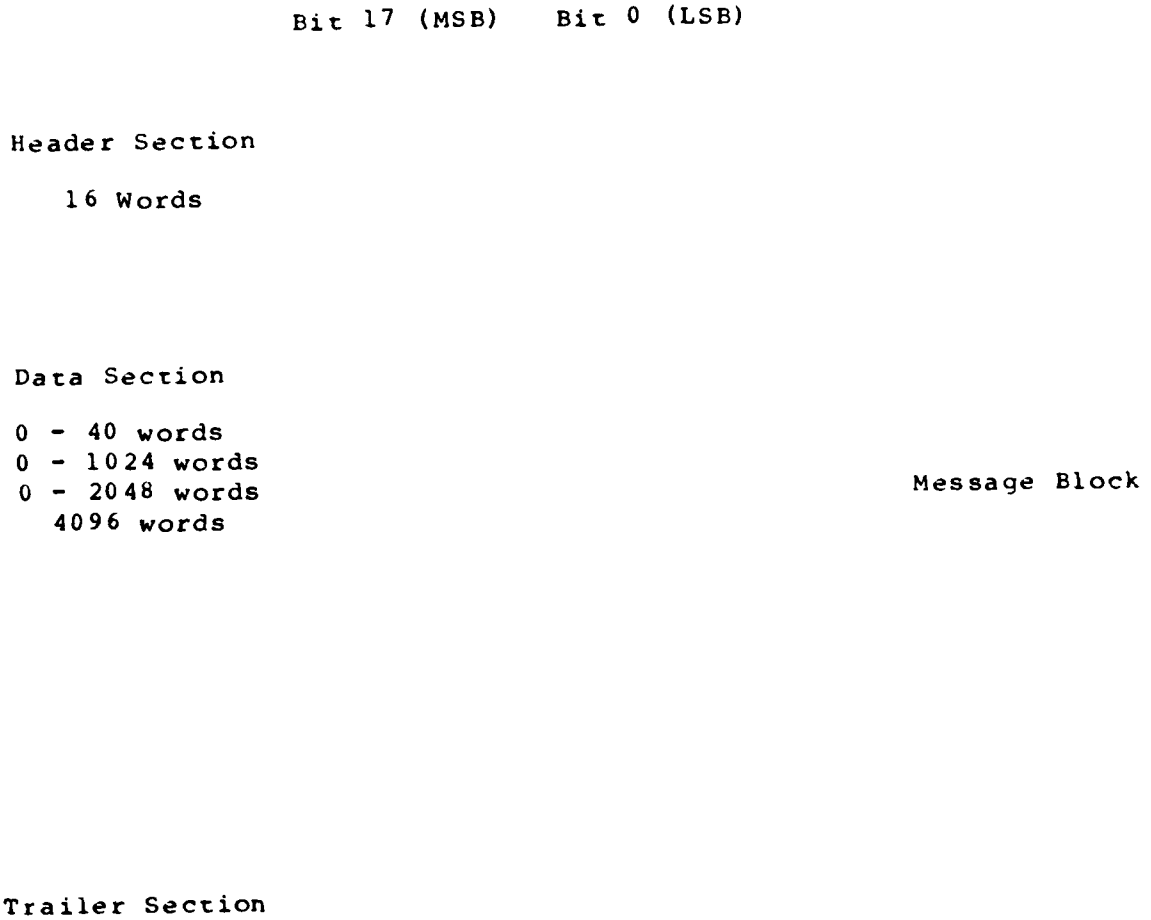


FIGURE 10. Digital Link Interface Message Block Format

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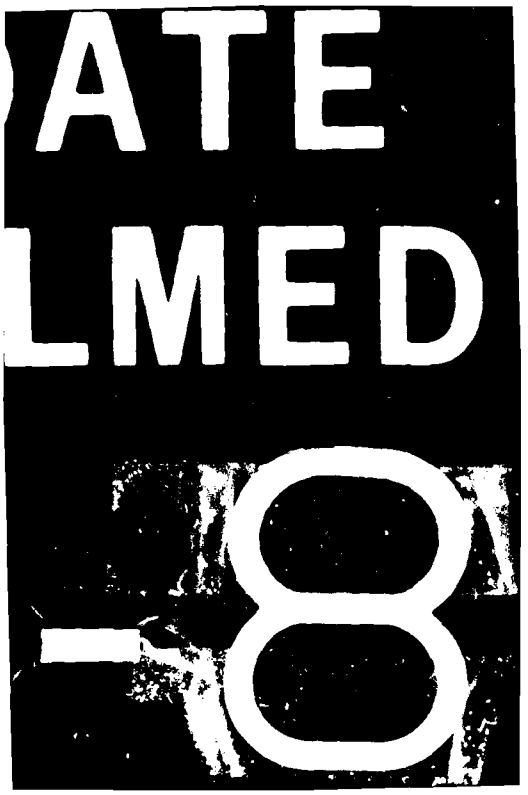
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